Logic Gates
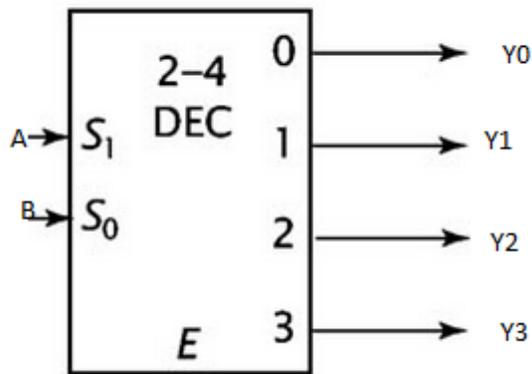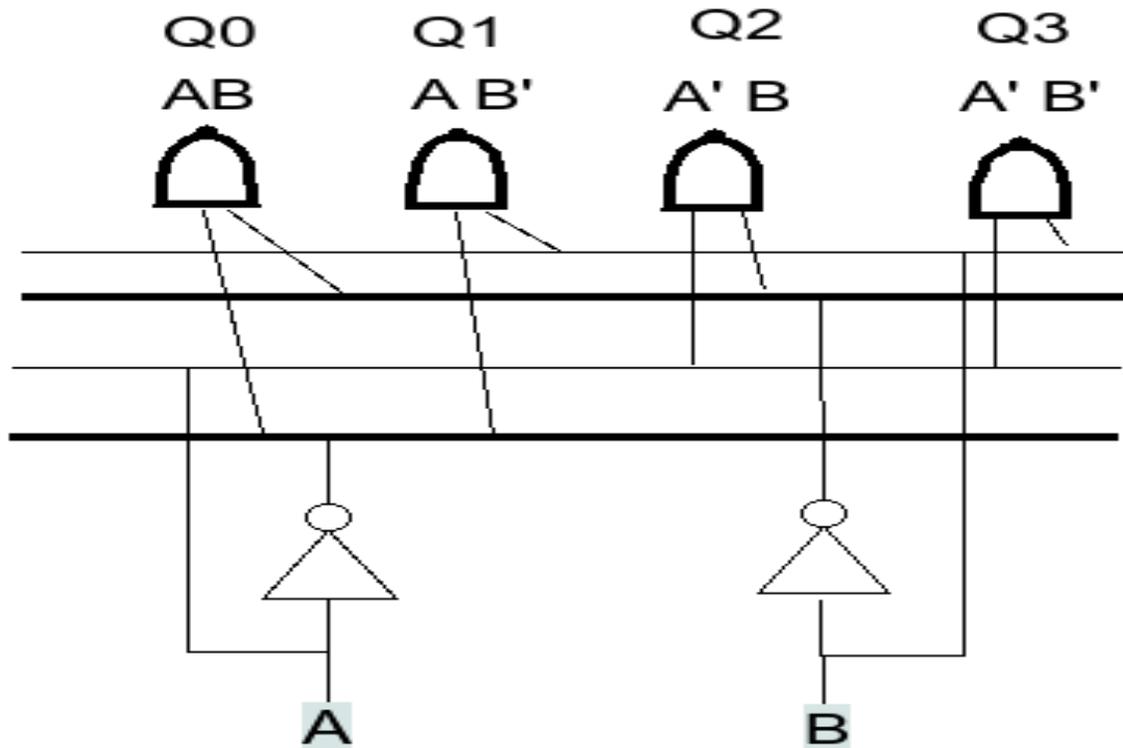
We wish to synthesize a 2 to 4 decoder with active outputs low.

What is active inputs low?

Decoder Theory compliments of
http://coep.vlab.co.in/?sub=28&brch=81&sim=609&cnt=1

Ready now to answer:

1. Establishing the truth table of the circuit.

A	B	Q0	Q1	Q2	Q3
0	**0**	**0**	**0**	**0**	**1**
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

***** 2. Determine output functions Y= f(A,B) A and B are the i

I really do not understand this question but I think the answer is:
f(Ai ,Bi) = (A*B)'
Generalized
f(A,B) = (A'*B')' Union (A'*B)' Union (A*B')' Union (A*B)'
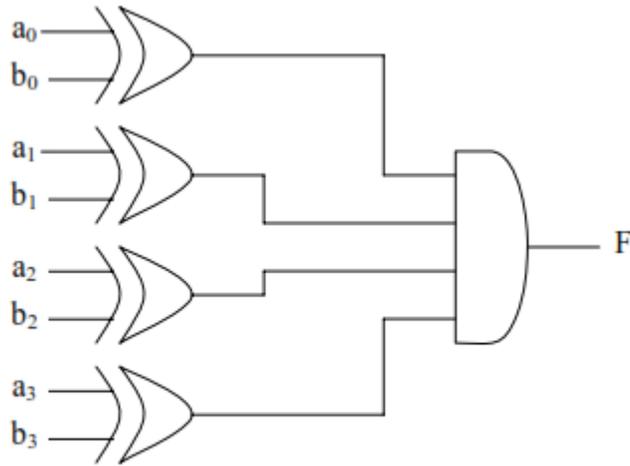   where A=B (A=i) (B=i)
f(A,B) = A'*A'
f(A,B) = A

??

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I need to talk about this and find further research.

Analyze the circuit below and define its role.

$(a0 + b0) * (a1 + b1) *(a2 + b2) * (a3 +b3) = F$ where + is an XOR since I have no xor symbol

a	b	Si
0	0	0
0	1	1
1	0	1
1	1	0

S0	S1	S2	S3	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0

1	1	1	0	0
1	1	1	1	1

Umm - it requires that all the sets of a and b are odd? 1 is in all the sets ab that a and b are opposite (inverse) of each other, or that only one is on.